February 1988

MM54C240/MM74C240 Inverting MM54C244/MM74C244 Non-Inverting Octal Buffers and Line Drivers with TRI-STATE® Outputs

General Description

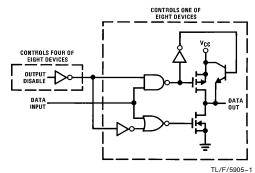
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state. For improved TTL input compatibility see MM74C941.

Features

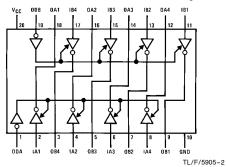
- Wide supply voltage range (3V to 15V)
- High noise immunity (0.45 V_{CC} typ)
- Low power consumption
- High capacitive load drive capability
- TRI-STATE outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package
- High speed 25 ns (typ.) @ 10V, 50 pF (MM74C244)

Logic and Connection Diagrams

MM54C240/MM74C240



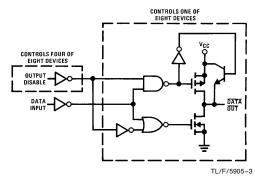
MM54C240/MM74C240 Dual-In-Line Package



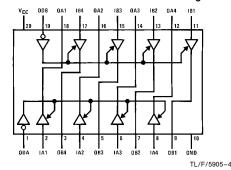
Top View

Order Number MM54C240 or MM74C240

MM54C244/MM74C244



MM54C244/MM74C244 Dual-In-Line Package



Top View

Order Number MM54C244 or MM74C244

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin

 $-0.3 \mbox{V to V}_{\mbox{CC}} + 0.3 \mbox{V}$

Operating Temperature Range MM54C240, MM54C244

 Storage Temperature Range

 -65°C to $+150^{\circ}\text{C}$

Power Dissipation

Dual-In-Line Small Outline 700 mW 500 mW

Operating V_{CC} Range Absolute Maximum V_{CC} 3V to 15V 18V

260°C

Lead Temperature (Soldering, 10 seconds)

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Тур | Max | Units |
|---------------------|--------------------------------------|---|---|--------|------------|--------|
| смоѕ то сі | MOS | | | | | |
| V _{IN(1)} | Logical "1" Input Voltage | $V_{CC} = 5V$ $V_{CC} = 10V$ | 3.5 8.0 | | | V V |
| V _{IN(0)} | Logical "0" Input Voltage | $V_{CC} = 5V$ $V_{CC} = 10V$ | | | 1.5 2.0 | V V |
| V _{OUT(1)} | Logical "1" Output Voltage | $V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$ | 4.5 9.0 | | | V V |
| V _{OUT(0)} | Logical "0" Output Voltage | $V_{CC} = 5V$, $I_O = 10 \mu A$ $V_{CC} = 10V$, $I_O = 10 \mu A$ | | | 0.5 1.0 | V V |
| loz | TRI-STATE Output Current | $V_{CC} = 10V, OD = V_{IH}$ | | | ±10 | μΑ |
| I _{IN(1)} | Logical "1" Input Current | V _{CC} = 15V, V _{IN} = 15V | | 0.005 | 1.0 | μΑ |
| I _{IN(0)} | Logical "0" Input Current | $V_{CC} = 15V, V_{IN} = 0V$ | -1.0 | -0.005 | | μΑ |
| Icc | Supply Current | V _{CC} = 15V | | 0.05 | 300 | μΑ |
| CMOS/LPTT | TL INTERFACE | | • | | | |
| V _{IN(1)} | Logical "1" Input Voltage | 54C, V _{CC} = 4.5V 74C, V _{CC} = 4.75V | V _{CC} - 1.5 V _{CC} - 1.5 | | | V V |
| V _{IN(0)} | Logical "0" Input Voltage | 54C, V _{CC} = 4.5V 74C, V _{CC} = 4.75V | | | 0.8 0.8 | V V |
| V _{OUT(1)} | Logical "1" Output Voltage | 54C, $V_{CC} = 4.5V$, $I_{O} = -450~\mu A$ 74C, $V_{CC} = 4.75V$, $I_{O} = -450~\mu A$ | $\begin{array}{c} V_{CC}-0.4 \\ V_{CC}-0.4 \end{array}$ | | | V V |
| | | $54C$, $V_{CC} = 4.5V$, $I_{O} = -2.2$ mA $74C$, $V_{CC} = 4.75V$, $I_{O} = -2.2$ mA | 2.4 2.4 | | | V V |
| V _{OUT(0)} | Logical "0" Output Voltage | $54C$, $V_{CC} = 4.5V$, $I_{O} = 2.2$ mA $74C$, $V_{CC} = 4.75V$, $I_{O} = 2.2$ mA | | | 0.4 0.4 | V V |
| OUTPUT DR | IVE (See 54C/74C Family Char | racteristics Data Sheet) (Short Circuit | Current) | | | |
| ISOURCE | Output Source Current (P-Channel) | $V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25^{\circ}C$ | -14 | -30 | | mA |
| | | $V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^{\circ}C$ | -36 | -70 | | mA |
| I _{SINK} | Output Sink Current (N-Channel) | $V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25^{\circ}C$ | 12 | 20 | | mA |
| | | $V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^{\circ}C$ | 48 | 70 | | mA |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

| Symbol | Parameter | Conditions | Min | Тур | Max | Units |
|---|---|--|-----|-----|-----|-------|
| t _{PD(1)} , t _{PD(0)} | Propagation Delay (Data In to Out) | | | | | |
| | MM54C240/MM74C240 | $V_{CC} = 5V, C_{L} = 50 \text{ pF}$ | | 60 | 90 | ns |
| | | $V_{CC} = 10V, C_{L} = 50 pF$ | | 40 | 70 | ns |
| | | $V_{CC} = 5V, C_L = 150 pF$ | | 80 | 110 | ns |
| | | $V_{CC} = 10V, C_L = 150 pF$ | | 60 | 90 | ns |
| | MM54C244/MM74C244 | $V_{CC} = 5V, C_{L} = 50 pF$ | | 45 | 70 | ns |
| | | $V_{CC} = 10V, C_{L} = 50 pF$ | | 25 | 50 | ns |
| | | $V_{CC} = 5V, C_L = 150 pF$ | | 60 | 90 | ns |
| | | $V_{CC} = 10V, C_L = 150 pF$ | | 40 | 70 | ns |
| t _{1H} , t _{0H} | Propagation Delay Output | $R_L = 1k, C_L = 50 pF$ | | | | |
| | Disable to High Impedance | $V_{CC} = 5V$ | | 45 | 80 | ns |
| | State (from a Logic Level) | $V_{CC} = 10V$ | | 35 | 60 | ns |
| t _{H1} , t _{H0} | Propagation Delay Output | $R_{L} = 1k, C_{L} = 50 pF$ | | | | |
| | Disable to Logic Level | V _{CC} = 5V | | 50 | 90 | ns |
| | (from High Impedance State) | $V_{CC} = 10V$ | | 30 | 60 | ns |
| t _{T(HL)} , t _{T(LH)} | Transition Time | $V_{CC} = 5V, C_{L} = 50 \text{ pF}$ | | 45 | 80 | ns |
| . , . , | | $V_{CC} = 10V, C_{L} = 50 pF$ | | 30 | 60 | ns |
| | | $V_{CC} = 5V, C_L = 150 pF$ | | 75 | 140 | ns |
| | | $V_{CC} = 10V, C_L = 150 pF$ | | 50 | 100 | ns |
| C _{PD} | Power Dissipation Capacitance (Output Enabled per Buffer) | (Note 3) | | | | |
| | MM54C240/MM74C240 | | | 100 | | pF |
| | MM54C244/MM74C244 | | | 100 | | pF |
| | (Output Disabled per Buffer) | | | | | |
| | MM54C240/MM74C240 | | | 10 | | pF |
| | MM54C244/MM74C244 | | | 0 | | pF |
| C _{IN} | Input Capacitance (Any Input) | $V_{IN} = 0V, f = 1 \text{ MHz}, T_A = 25^{\circ}\text{C}$ | | 10 | | pF |
| Co | Output Capacitance (Output Disabled) | $V_{IN} = 0V, f = 1 \text{ MHz}, T_A = 25^{\circ}\text{C}$ | | 10 | | pF |

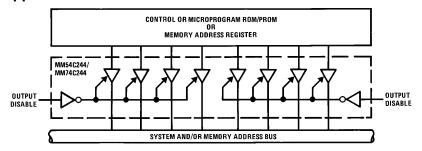
^{*}AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

Typical Application



TL/F/5905-5

Truth Tables

MM54C240/MM74C240

| ODA | IA | OA |
|-----|----|----|
| 1 | Х | Z |
| 1 | Х | Z |
| 0 | 0 | 1 |
| 0 | 1 | 0 |

| ODB | IB | ОВ |
|-----|--------|----|
| 1 | Х | Z |
| 1 | X X | Z |
| 0 | 0 | 1 |
| 0 | 1 | 0 |

MM54C244/MM74C244

| ODA | IA | OA |
|-----|----|----|
| 1 | Х | Z |
| 1 | X | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |

1 = High

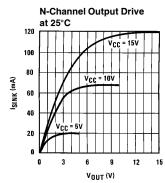
0 = Low

X = Don't Care

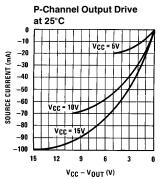
Z = TRI-STATE

| ODB | IB | ОВ |
|-----|----|----|
| 1 | X | Z |
| 1 | Х | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |

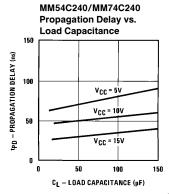
Typical Performance Characteristics



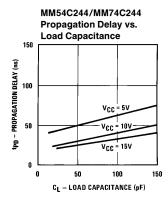
TL/F/5905-6



TL/F/5905-7



TL/F/5905-8

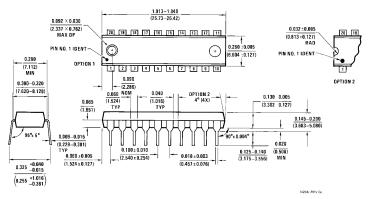


TL/F/5905-9

AC Test Circuits and Switching Time Waveforms CMOS to CMOS t_{pd0}, t_{pd1} ν_{CC} ν_{IN} vcc TL/F/5905-10 VOUT TL/F/5905-11 t_{1H} and t_{H1} t_{1H} t_{H1} vcc-DISABLE 0.5 V_{CC} DISABLE -0.5 V_{CC} tH1 t_{1H} DISABLE ۷он OUTPUT OUTPUT 0.5 V_{OH} TL/F/5905-12 TL/F/5905-13 Note: V_{OH} is defined as the DC output high voltage when the device is loaded with $t_{0H} \, \text{and} \, t_{H0}$ t_{OH} t_{H0} 0.5 V_{CC} DISABLE DISABLE - 0.5 V_{CC} toH INPUT vcc v_{cc} 0.5 (V_{CC} - V_{OL}) OUTPUT OUTPUT DISABLE VOL-V_{OL} TL/F/5905-14 0.1 ($V_{CC} - V_{OL}$) TL/F/5905-15 Note: V_{OL} is defined as the DC output low voltage when the device is loaded with a 1 $k\Omega$ resistor to V_{CC} Note: Delays measured with input $t_{\text{r}},\,t_{\text{f}}\,\leq\,$ 20 ns.

Physical Dimensions inches (millimeters) 0.985 20 19 18 17 16 15 14 13 12 11 1 2 3 4 5 6 7 8 9 10 0.005 - 0.020 (0.127 - 0.508) RAD TYP 0.037 ± 0.005 (0.940 ± 0.127) 0.005 (0.127) MIN 0.290 - 0.320 (7.366 - 8.128) 0.020 - 0.060 (0.508 - 1.524) GLASS SEALANT 0.125 - 0.200 (3.175 - 5.080) $\frac{0.008 - 0.012}{(0.203 - 0.305)}$ 0.060 (1.524) MAX BOTH ENDS 0.018±0.003 (0.457±0.076) 0.310 - 0.410 (7.874 - 10.41)

Ceramic Dual-In-Line Package (J) Order Number MM54C240J, MM54C244J, MM74C240J or MM74C244J See NS Package Number J20A



Molded Dual-In-Line Package (N) Order Number MM54C240N, MM54C244N, MM74C240N or MM74C244N See NS Package Number N20A

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- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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